CLAIMS

1. (Previously presented) A circuit comprising:

a first device coupled with a first bus, wherein the first device is not compliant with a standard, the first device containing data, wherein the data is not operational for the circuit with a device that is not compliant with the standard;

a second device coupled with a second bus, wherein the second device is compliant with the standard, the second device to be associated with the data from the first device, the association of the second device with the data from the first device enabling data from the first device to be utilized according to the standard; and

a memory to receive the data from the first device.

2. (Previously Presented) The circuit of claim 1, further comprising a plurality of devices coupled with the second bus, wherein each of the plurality of devices is compliant with the standard, and wherein the plurality of devices includes the second device.

3. (Previously Presented) The circuit of claim 2, further comprising a controller coupled with the first bus and the second bus to scan the plurality of standard devices to identify the second device.

4. (Original) The circuit of claim 1, wherein the second device comprises a function of a physical device.

5. (Original) The circuit of claim 1, wherein the first device comprises flash memory.

6. (Original) The circuit of claim 1, wherein the data comprises an operating system.

7. (Original) The circuit of claim 6, wherein the data includes a boot loader, the boot loader being stored as an option-ROM for the first device.

8. (Previously Presented) The circuit of claim 1, wherein the standard comprises a PCI (peripheral component interconnect) specification, and wherein the second bus is a PCI bus.

9. (Previously presented) A method comprising:

identifying a peripheral device that is coupled with a first bus, the peripheral device being a standard peripheral device according to a standard;

associating the standard peripheral device with data of a non-standard peripheral device that is coupled with a second bus, wherein the data is not operational with a non-standard peripheral device; and

based on the association of the standard peripheral device with the data of the non-standard peripheral, dispatching the data of the non-standard device to memory as data in accordance with the standard of the standard peripheral device.

10. (Previously Presented) The method of claim 9, wherein identifying the standard peripheral device comprises choosing the standard peripheral device from a plurality of standard peripheral devices that are coupled with the first bus.

11. (Original) The method of claim 10, wherein choosing the standard peripheral device comprises pre-selecting the standard peripheral device before commencing operations.

12. (Previously Presented) The method of claim 10, wherein choosing the standard peripheral device comprises scanning the plurality of standard peripheral devices coupled with the first bus to identify a suitable device.

13. (Previously Presented) The method of claim 9, wherein the standard comprises a PCI (peripheral component interconnect) specification.

14. (Original) The method of claim 9, wherein the data comprises an operating system.

15. (Original) The method of claim 14, wherein the data includes a boot loader, the boot loader being stored as an option-ROM.

16. (Previously presented) A computer system comprising:

a processor;

a first bus, the first bus being in compliance with a standard;

a first device that is not compliant with a standard, the first device being coupled with a second bus, the first device containing data, wherein the data is not

operational for the computer system with a device that is not compliant with the standard;

a plurality of devices in compliance with the standard, each of the plurality of devices being coupled with the second bus, the plurality of devices including a second device to be the data from the first device, the processor recognizing the data as being data in accordance with the standard because of the association of the second device with the data; and

a memory to receive the data from the first device.

17. (Original) The computer system of claim 16, wherein the computer system is an embedded system.

18. (Previously Presented) The computer system of claim 16, further comprising a controller coupled with the first bus and the second bus to scan the plurality of devices in compliance with the standard to identify the second device.

19. (Original) The computer system of claim 16, wherein the plurality of devices includes one or more functions of a physical device.

20. (Original) The computer system of claim 16, wherein the first device comprises flash memory.

21. (Original) The computer system of claim 16, wherein the data comprises an operating system.

22. (Previously Presented) The computer system of claim 16, wherein a portion of the data is stored as an option-ROM for the first device.

23. (Original) The computer system of claim 16, wherein the standard comprises a PCI (peripheral component interconnect) specification.

24. (Previously presented) A machine-readable medium having stored thereon data representing sequences of instructions that, when executed by a processor, cause the processor to perform operations comprising:

identifying a standard peripheral device on a first bus;

associating the standard peripheral device with data contained in a non-standard peripheral device, wherein the data is not operational with a non-standard peripheral device; and

based on the association of the standard peripheral device with the data of the non-standard peripheral, dispatching the data of the non-standard device to memory as data in accordance with the standard of the standard peripheral device.

25. (Previously Presented) The medium of claim 24, wherein identifying the standard peripheral device comprises choosing the standard peripheral device from a plurality of standard peripheral devices on the first bus.

26. (Original) The medium of claim 25, wherein choosing the standard peripheral device comprises pre-selecting the standard peripheral device before commencing operations.

27. (Previously Presented) The medium of claim 25, wherein choosing the standard peripheral device comprises scanning the plurality of standard peripheral devices on the first bus to identify a suitable device.

28. (Previously Presented) The medium of claim 24, wherein the standard comprises a PCI (peripheral component interconnect) specification.

29. (Original) The medium of claim 24, wherein the data comprises an operating system.

30. (Original) The medium of claim 29, wherein the data includes a boot loader, the boot loader being stored as an option-ROM.

31. (Previously Presented) The apparatus of claim 3, further comprising a second controller coupled with the controller and the memory, wherein the memory receives the data via the second controller.

32. (Previously Presented) The method of claim 12, wherein the scanning of the plurality of standard peripheral devices is performed by a first controller that is coupled with the first bus and the second bus.

33. (Previously Presented) The method of claim 32, wherein the dispatching of the data to memory comprises transferring the data to memory via a second controller that is coupled with the memory and the first controller.

34. (Previously Presented) The computer system of claim 18, further comprising a second controller coupled with the controller and the memory, wherein the memory receives the data via the second controller.

35. (Previously Presented) The medium of claim 25, wherein the choice of the standard peripheral devices from the plurality of standard peripheral devices is

performed by a first controller that is coupled with the first bus and the second bus.

36. (Previously Presented) The method of claim 35, wherein the dispatching of the data to memory comprises transferring the data to memory via a second controller that is coupled with the memory and the first controller.